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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER	
ELLIS, KEVIN L	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 04/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/803,452	RAKVIC ET AL.	
	Examiner	Art Unit	
	Kevin L. Ellis	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13 and 17-25* is/are rejected.

7)☒ Claim(s) *14-16 and 26-28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/28/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1. Claims 1-28 are presented for examination.

2. Information disclosed and listed on PTO 1449 has been considered.

Claim Objections

3. Claim 1 is objected to because of the following informalities:

A) Claim 1 recites: "the respective cache memory;" the ';' at the end of the line should be changed to a period '.'

Double Patenting

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 1-13 and 17-25 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-37 of U.S. Patent No. 6,668,306. Although the conflicting claims are not identical, they are not patentably distinct from each other because both sets of claims are directed to providing multiple caches for a CPU wherein the caches store data based upon the vitality of the data being loaded.

Claim Rejections – 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

7. Claims 1, 2, and 17 are rejected under 35 U.S.C. § 102(e) as being anticipated by Holmberg et al., U.S. Patent 6,865,736.

A) As to claims 1 and 17, Holmberg et al. discloses the invention as claimed. There is a system comprising a CPU (Fig 1a Ref 11), one or more cache memories coupled to the CPU (see Col 3 Lines 18-22 and 39-40), each to store only data for loads to be processed by the CPU that have a vitality matching the latency associated with the respective cache memory (see Col 3 Lines 1-17). As for the identifying of claim 17, see Col 3 Lines 17-65.

B) As to claim 2, Holmberg et al. teaches having a vital load cache memory and a non-vital load cache memory (Col 13 Lines 51-67).

8. Claims 1-13 and 17-25 are rejected under 35 U.S.C. § 102(a) as being anticipated by Rakvic et al., U.S. Patent 6,668,306.

A) As to claims 1-3, Rakvic et al. discloses the invention as claimed. There is a system comprising a CPU (Fig 2 Ref 130 and Fig 3 Ref 315) and one or more cache memories, coupled to the CPU (Fig 2 Ref 225 and Fig 3 Ref 230-1 to 230-4), each to store only data for loads to be processed by the CPU that have a vitality matching the latency associated with the respective cache memory (see Col 3 Lines 31-65 and Col 4 Lines 30-45). Rakvic et al. discloses the multiple caches that would read upon the vital, semi-vital, and non-vital caches.

B) As to claim 4, the caches would be accessed in parallel (see Fig 2).

C) As to claims 5-7, the different types of loads (vital, semi-vital, non-vital) are directly assigned to the different caches (see Col 3 Lines 31-65 and Col 4 Lines 30-45) and the assignment can be determined by a compiler (see Col 4 Lines 7-10).

D) As to claims 8-10, Rakvic et al. teaches having a caches for loads that are processed within one clock cycle, three clock cycles, and four clock cycles (see Fig 3 and Col 4 Lines 30-45).

E) As to claims 11-12, Rakvic et al. states no limitation on the sizes of the cache memory and could thus met the claimed sizes.

F) As to claim 13, the first and third cache memories do operate at the same level in the hierarchy (see Fig 2 and 3).

G) As to claims 17-20, these limitations have been addressed with respect to the rejections above and the apply here as well.

H) As to claim 21, Rakvic et al. discloses the invention as claimed. There is a computer system comprising a CPU (Fig 2 Ref 130 and Fig 3 Ref 315), a first cache memory (Fig 3 Ref 230-1), a second cache memory (Fig 3 Ref 230-3), a third cache memory (Fig 3 Ref 230-4), and a main memory (Fig 1 Ref 135 and Col 4 Lines 50-53). As for the claimed "chipset", this can be read on a memory controller for the computer system which would be an inherent part of the system. Since the computer system has a main memory, there must be some controller to control access to the main memory.

I) As to claim 22, the caches would be accessed in parallel (see Fig 2).

J) As to claims 23 and 24, the different types of loads (vital, semi-vital, non-vital) are directly assigned to the different caches (see Col 3 Lines 31-65 and Col 4 Lines 30-45)

that are for loads that are processed within one clock cycle, three clock cycles, and four clock cycles (see Fig 3 and Col 4 Lines 30-45).

K) As to claim 25, the first and second cache memories do operate at the same level in the hierarchy (see Fig 2 and 3).

Claim Rejections – 35 USC § 103

9. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 3-13 and 18-21 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Holmberg et al., U.S. Patent 6,865,736.

A) As to claims 3 and 18, Holmberg et al. discloses the invention substantially as claimed. However, Holmberg et al. does not teach the third cache memory for storing semi-vital loads. Since Holmberg et al. teaches having a system with multiple caches (the first and second cache), it would have been obvious to one having ordinary skill in the art at the time the invention was made to extend the system to have additional cache memories. Holmberg et al. teaches having one cache memory for vital loads (i.e. loads that are low latency) and having another cache memory or other loads, it would be obvious that there could be additional cache memories for various levels of latency, for the same reason as providing the one cache memory for low latency (optimized use of the cache memory). Accordingly, it would have been obvious to one having ordinary skill in

the art at the time of the invention to have extend the system of Holmberg et al. to have the third cache memory for storing semi-vital loads for the reasons stated above.

B) As to claim 5, the various loads would be assigned to the caches based upon their vitality, this is taught by Holmberg et al. where vital loads are sent to the first cache memory.

C) As to claim 6, the loads are assigned statically (see Col 3 Lines 7-13).

D) As to claim 7, Holmberg et al. discusses that the assignment could be determined by a compiler (see Col 2 Lines 9-23 and Col 12 Lines 41-49).

E) As to claims 8-10, Holmberg et al. discloses the invention substantially as claimed. However, Holmberg et al. does not specifically give clock cycles that would make a load a vital, semi-vital, or non-vital load. The selection of the number of clock cycles that would make a load a vital, semi-vital, or non-vital load would be vary dependent upon the system and the application running on that specific system as different numbers would give different levels of performance increases. Accordingly, it would have been obvious to one having ordinary skill in the art at the time of the invention that the number of clock cycles to distinguish the various types of load would vary and could be one for vital, three for semi-vital, and at least four for non-vital as claimed.

F) As to claims 11-13, the cache memories of Holmberg et al. can be of varying size and operate at various levels in the hierarchy such as those claimed.

G) As to claims 19-20, Holmberg et al. discloses performing a profile of the instructions to determine which cache memory they should be assigned to (see Col 3 Lines 17-65).

H) As to claim 21, Holmberg et al. discloses the invention substantially as claimed. There is a computer system comprising a CPU (Fig 1a Ref 11), a first cache to store data for vital loads (see Col 3 Lines 1-40), a third cache memory to store non-vital loads (see Col 13 Lines 51-67), a chipset coupled to the CPU (Fig 1a Ref 14), and a main memory coupled to the chipset (Fig 1a Ref 16). However, Holmberg et al. does not teach the second cache memory for storing semi-vital loads. Since Holmberg et al. teaches having a system with multiple caches (the first and third cache), it would have been obvious to one having ordinary skill in the art at the time the invention was made to extend the system to have additional cache memories. Holmberg et al. teaches having one cache memory for vital loads (i.e. loads that are low latency) and having another cache memory or other loads, it would be obvious that there could be additional cache memories for various levels of latency, for the same reason as providing the one cache memory for low latency (optimized use of the cache memory). Accordingly, it would have been obvious to one having ordinary skill in the art at the time of the invention to have extend the system of Holmberg et al. to have the second cache memory for storing semi-vital loads for the reasons stated above.

Allowable Claims

11. Claims 14-16 and 26-28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin L. Ellis whose telephone number is 571-272-4205. The examiner can normally be reached on weekdays from 6:00AM-2:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone numbers for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Kevin L. Ellis
Primary Examiner
March 29, 2006